AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph [7] on pages 2-3 with the following amended paragraph:

[7] The built-in CPU or serial communication controller 11 is an apparatus for processing data transmitted from a communication network and performing serial communication control function. The multi-protocol transceiver 12 is an apparatus capable of transmitting and receiving more than two protocol signals, which can transmit and receive digital signals, and can receive signals during transmission if a transmission frequency and a receiving frequency are different from each other.

Please replace paragraph [11] on page 3 with the following amended paragraph:

[11] The built-in CPU or serial communication controller 11 sends a chip select (CS) signal to the data buffer 14 in order to recognize the H/W protocol from the cable connected to a wide area communication network during the initialization process. The data buffer 14 enabled upon receipt of the CS signal, and discriminates a H/W protocol through a mode [2:0] line to send the same to the built-in CPU or serial communication controller 11. The built-in CPU or serial communication controller 11 completes initialization by executing a program corresponding to the transmitted protocol mode.

Please replace paragraphs [32]-[34] on page 10 with the following amended paragraphs:

[32] The built-in CPU or serial communication controller 21 ~~functions as a serial communication controller for processing~~ processes data transmitted from a communication network and ~~executing~~ executes a program according to a H/W protocol.

[33] The multi-protocol transceiver 22 is an apparatus that makes it possible to transmit and receive more than two protocols between the built-in CPU or serial communication controller 21 and the connector 23. The connector 23 is an apparatus for providing a connection port between the router and DCE.

[34] The PLD 24 is an apparatus capable of programming the corresponding operation logic for the execution of a particular operation. The ~~PDL~~ PLD 24 has an operation logic programmed to sense whether the connector 23 is in the disconnection state or in the connection state, or what a H/W protocol is like, and informs the built-in CPU or serial communication controller 21 of the same. Pull-up resistors R1 26 and R2 27 connected to the PLD 24 are connected to a positive power voltage (Vcc), and prevent erroneous operation when an operation signal is not transmitted.

Please replace paragraphs [36]-[39] on pages 10-12 with the following amended paragraphs:

[36] An operation of the preferred embodiment of the thusly configured apparatus will now be described. There are occasions when cables are replaced or a H/W protocol is changed

during the operation of the router. In such a situation, the preferred embodiment is devised to automatically ~~recognizes~~ recognize the change and ~~not~~ need not re-initialization.

[37] When changing cables, the instant that the connector 23 at the router is disconnected with the connector 33 at DCE, the PLD 24 preferably senses the change in the state of the connector 23 though a cable state sensing line [[27]], and discriminates a H/W protocol through a protocol mode line [[26]]. In addition, to inform the built-in CPU or serial communication controller 21 of the change in the state of the connector 23, the PLD 24 transmits an interrupt request (IRQ) signal to the CPU or serial communication controller 21. The built-in CPU or serial communication controller 21 then sends an acknowledgment (ACK) signal in response to the IRQ, and sends a CS signal requesting a H/W protocol mode value transmission. After receiving the protocol mode information from the PLD 24, the built-in CPU or serial communication controller 21 normalizes communication environments and system operation by initializing parts of the apparatus.

[38] The sensing of the change in the state of the connection cable will now be described in more detail.

[39] A hole of the connector 23 at the router connected to the cable state sensing line [[27]] is engaged with a corresponding pin while coupling with the connector [[33]] 23 at the DCE. In the preferred embodiment, pin P4 is a pin connected to ground all the time, regardless of the type of the connector. Thus, the open state of pin P4 logically represents no cable connection, and has a logical high voltage value set by the pull-up resistor R2 27 of the cable

state sensing line [[27]]. The ground state has a logical low voltage value representing a cable connection between W4 and P4.